



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/714,745

Confirmation No. 4672

First Inventor: Brian J. Campbell

Filed: 11/17/2003

Art Unit: 2819

Examiner: Tan, Vibol

Title: Dynamic Scan Circuitry For B-Phase

Continuation of 10/127,259; filed 04/22/2002; now US Patent 6,686,775

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant submits the attached Information Disclosure Statement and requests the Examiner to consider the listed references. All of the references noted on this IDS were submitted on Form PTO-1449 by the Applicant or cited by the Examiner in the parent case, Application No. 10/127,259; filed 04/22/2002; now U.S. Patent 6,686,775. Thus, copies of the references are in the parent case.

If there are any fee shortages related to this submission, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

GARLICK, HARRISON & MARKISON, LLP
(Customer No. 34,399)

Date: 8-13-04

By: William W. Kidd

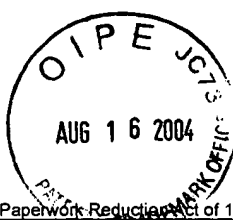
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STATEMENT BY APPLICANT**

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Complete if Known

Application Number	10/714,745
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Examiner Name	Tan, Vibol
Attorney Docket Number	BP2243CON

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U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
		US- 5,459,736	10/17/95	Nakamura	
		US- 5,689,517	11/18/97	Ruparel	
		US- 4,061,933	12/6/77	Schroeder et al.	
		US- 5,831,462	11/3/98	Witt et al.	
		US- 6,223,282	4/24/01	Kang	
		US- 6,318,911	11/20/01	Kitahara	
		US- 6,247,134	6/12/01	Sproch et al.	
		US- 6,272,667	8/7/01	Minami et al.	
		US- 5,815,725	9/29/98	Feierbach	
		US- 6,411,152	6/25/02	Dobberpuhl	
		US- 5,748,015	5/5/98	Tam	
		US- 5,838,179	11/17/98	Schmidt	
		US- 6,297,670	10/2/01	Chao et al.	
		US- 6,535,036	3/18/03	Dobberpuhl	
		US- 6,429,689	8/6/02	Allen et al.	
		US- 6,057,711	5/2/00	Sessions	
		US- 5,870,411	2/9/99	Durham et al.	
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

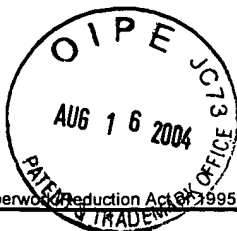
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		Country Code ³ *Number ⁴ *Kind Code ⁵ (if known)				
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Stephany et al., "FP15.5: A 200 MHz 32b 0.5W CMOS RISC Microprocessor," Digital Semiconductor, Austin TX, IEEE, 1998, pp. 15.5-1 to 15.5-9.	
		Santhanam et al., "SA 18.6: A Low-Cost 300MHz RISC CPU with Attached Media Processor," Digital Equipment Corp., Palo Alto, CA, IEEE, 1998, pp. 18.6-1 to 18.6-9.	
		Montanaro et al., "A 160-MHz, 32-b, 0.5-W CMOS RISC Microprocessor," IEEE Journal of Solid-State Circuits, vol. 31, No. 11, Nov. 1996, 12 pages.	
		Weiss et al., "The On-Chip 3MB Subarray Based 3rd Level Cache on an Itanium Microprocessor," IEEE, ISSCC 2002, Session 6, 3 pages.	
		Josephson et al., "Test Methodology for the McKinley Processor," IEEE, ITC International Test Conference, Paper 21.1., 2001, pp. 578-585.	
		Santhanam et al., Presentation for: "A 1GHz Power Efficient Single Chip Multiprocessor System For Broadband Networking Applications," Broadcom Corp., Jun. 14, 2001, 19 pages.	
		Santhanam et al., "A 1GHz Power Efficient Single Chip Multiprocessor System For Broadband Networking Applications," Broadcom Corp., Jun. 14, 2001, 4 pages.	

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